

CALIBRATION TECHNIQUES FOR FREQUENCY SYNTHESIZERS

ABSTRACT

In one embodiment, this disclosure describes a frequency synthesizer for use in a wireless communication device, or similar device that requires precision frequency synthesis but small amounts of noise. In particular, the frequency synthesizer may include a phase locked loop (PLL) and an integrated voltage controlled oscillator (VCO). The frequency synthesizer may implement one or more calibration techniques to quickly and precisely calibrate the VCO. In this manner, the analog gain of the VCO can be significantly reduced, which may improve performance of the wireless communication device. Also, the initial state of the PLL may be improved to reduce lock time of the PLL, which may enhance performance of the wireless communication device.

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